IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl. No.	:	10/681,068	Confirmation No. : 8619
Appellant	:	Andrew S. Hildebrant, et al.	
Filed	:	October 7, 2003	
TC/A.U.	:	3714	
Examiner	:	Frank M. Leiva	
Docket No.	:	10030549-1	

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

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APPEAL BRIEF

Dear Sir:

This Appeal Brief is submitted in response to the Examiner's Office Action mailed May 8, 2008.

Appellants filed a Notice of Appeal on August 8, 2008.

Real Party in Interest

The real party in interest is Verigy (Singapore) Pte. Ltd., a Singapore limited liability company.

Related Appeals and Interferences

The rejections of the claims in United States patent application no. 10/666,024 have been appealed to the Board of Patent Appeals and Interferences. The decision on this appeal, when made, could be relevant to the appeal of the rejections of the claims in the instant application.

Status of Claims

Claims 1-17 are pending, all of which stand rejected. The rejections of claims 1-17 are appealed.

A copy of the claims is attached as a Claims Appendix to this Appeal Brief.

Status of Amendments

No amendments were made to the claims subsequent to final rejection. All amendments have been entered.

Summary of Claimed Subject Matter

In a first embodiment (claim 1) a machine-executable method comprises 1) reading a test file having a plurality of test vectors (p. 5, lines 10-18; FIG. 2, 200), 2) determining a required memory needed to execute the plurality of test vectors (p. 5, line 19 - p. 6, line 13; FIG. 2, 205), and 3) using the required memory to estimate a cost to execute the test vectors (p. 6, lines 14-20; FIG. 2, 210).

In a second embodiment (claim 8), a system (p. 4, lines 3-4; FIG. 1, 100) comprises 1) logic (FIG. 1, 102) to read a test file having a plurality of test vectors (p. 4, lines 5-6; p. 5, lines 10-18) and to determine a required memory needed to execute the plurality of test vectors (p. 4, lines 5-7; p. 5, line 19 - p. 6, line 13), and 2) a billing predictor (p. 4, lines 8-14; p. 6, lines 14-20; FIG. 1, 104), communicatively coupled to the logic, to use the required memory to estimate a cost to execute the test vectors.

In a third embodiment (claim 13), one or more machine-readable mediums have sequences of instructions stored thereon (p. 9, lines 5-10). When executed by a machine, the sequences of instructions cause the machine to perform the following actions: 1) read a test file having a plurality of test vectors (p. 5, lines 10-18; FIG. 2, 200); 2) determine a required memory needed to execute the plurality of test vectors (p. 5, line 19 - p. 6, line 13; FIG. 2, 205); and 3) use the required memory to estimate a cost to execute the test vectors (p. 6, lines 14-20; FIG. 2, 210).

Grounds of Rejection to be Reviewed on Appeal

1. Whether claims 1-17 should be provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-6 and 10-13 of copending application no. 10/666,024.

2. Whether claims 1-17 should be rejected under 35 USC 103(a) as being unpatentable over Williams et al. (US 2002/0093356 A1) in view of Ohara et al. (US 2002/0143418 A1).

Argument

1. Should claims 1-17 be provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-6 and 10-13 of copending application no. 10/666,024.

Appellants believe this rejection is moot as a result of their submission of an appropriate terminal disclaimer on August 8, 2008.

2. Claims 1-17 should not be rejected under 35 USC 103(a) as being unpatentable over Williams et al. (US 2002/0093356 A1; hereinafter "Williams") in view of Ohara et al. (US 2002/0143418 A1; hereinafter "Ohara").

A. Claims 1, 2, 5, 8, 9 & 12-14:

With respect to claim 1, the Examiner asserts that Williams teaches the steps of "reading a test file having a plurality of test vectors" and "determining a required memory needed to execute the plurality of test vectors" because:

> . . .Williams discloses. . .reading and storing the plurality of vectors in memory 1 and analysis [sic] the vector data to reduce (determined) the required memory for testing each vector.
>
> 5/8/2008 Office Action, p. 5, sec. 8 (referencing the teachings of Williams' ¶ [0014]).

For the Board's convenience, the entirety of Williams' paragraph [0014] is reproduced below:

> [0014] A method and circuit are described herein for testing an integrated circuit device using intelligent test vector formatting that reduces the memory required to store test patterns and also provides an encryption vehicle for the test patterns. The novel circuit includes a first memory that stores a test vector mask. The test vector mask is a sequence of bits that indicates if corresponding test vector data is deterministic or random. The test vector data

> used by the present invention contains a portion that is deterministically generated by automatic test pattern generation (ATPG) software and a portion that is random. A first data value of the mask indicates deterministic data and a second data value of the mask indicates random data. A second memory contains a sequence of bits that represent the deterministic test vector data. The first and second memory could be separate locations of the same memory device. Alternative variations of this method prefix the positions of deterministic data and random data such that the mask information is minimized to represent the encoded positions.

Appellants agree with the Examiner's assertion that Williams teaches "reading a test file having a plurality of test vectors". However, appellants do not agree with the Examiner's assertion that Williams teaches "determining a required memory needed to execute the plurality of test vectors".

The Examiner equates appellants' step of ***determining*** a required memory with Williams' step of ***reducing*** a required memory. However, the two steps are not the same, and appellants assert that ***reducing*** a required memory in no way teaches or suggests a need to ***determine*** a required memory.

Williams states in paragraph [0043] that, "An advantage of the embodiment of the present invention, as shown in FIG. 2, is that the memory required for storing the test patterns is reduced." Williams also states in this paragraph that the reduction may typically be on the order of 9:1. Presumably, both large and small numbers of test patterns might be compressed (or reduced) on the order of 9:1. However, after compression (or reduction), how much memory is required to execute the test patterns? Although "less" memory may be required for a smaller number of compressed test patterns, appellants believe it clear that a larger number of compressed test patterns will require "more" memory. But in either case, how much memory is required? Though Williams teaches that the memory needed to store a number of test patterns can be ***reduced*** by an arbitrary or estimable factor via compression, Williams provides absolutely no teaching or suggestion that 1) the "required memory needed to execute the plurality of test vectors", or 2) the required memory needed to store a compressed/reduced set of test patterns, should actually be ***determined***.

For the above reasons, appellants believe it is clear that Williams fails to teach the second step of their claim 1. This being the case, Williams necessarily fails to teach the step of "using the required memory to estimate a cost to execute the test vectors". That is, Williams cannot teach how to *use* the "required memory" if Williams does not even disclose how to *determine* the "required memory".

With respect to claim 1's step of "using the required memory to estimate a cost to execute the test vectors", the Examiner admits that Williams fails to teach this step. However, the Examiner notes that:

> . . .Ohara on the other hand teaches an automated method for calculating project costs which when applied to the Williams invention would use the calculated required memory to estimate a cost to execute the test vectors.
>
> 5/8/2008 Office Action, p. 5, sec. 8.

Although Ohara discloses a "product cost variance analysis system and control method" (*see*, e.g., Title; Abstract), appellants cannot find any mention by Ohara that its disclosed systems and methods should be applied to "test vectors" or memories. Nonetheless, the Examiner asserts that it would be obvious to combine Ohara's teachings with Williams' because Ohara's method for calculating project costs could be used on Williams' calculation of a "required memory" to estimate the cost to execute a plurality of test vectors. Yet, as already discussed, Williams never teaches (or even suggests) that the "required memory needed to execute the plurality of test vectors" should be calculated (or determined). This being the case, appellants cannot think of any reason why one of ordinary skill in the art would be motivated to combine Williams' and Ohara's teachings.

For the above reasons, claim 1 is believed to be allowable over the teachings of Williams and Ohara - taken alone, or in combination.

Claims 2 & 5 are believed to be allowable, at least, because they depend from claim 1.

Claim 8 is believed to be allowable, at least, for reasons similar to why claim 1 is believed to be allowable.

Claims 9 & 12 are believed to be allowable, at least, because they depend from claim 8.

Claim 13 is believed to be allowable, at least, for reasons similar to why claim 1 is believed to be allowable.

Claim 14 is believed to be allowable, at least, because it depends from claim 13.

B. Claims 3, 4, 10, 11, 15 & 16:

Claims 3 & 4 are believed to be allowable, in one respect, because they depend from claim 1. Claims 3 & 4 are also believed to be separately allowable because they respectively recite "determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board" and "determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin".

In support of the rejections of claim 3, the Examiner asserts that Williams discloses determining the required memory needed for each of a plurality of boards and pins in fig. 3 and paragraph [0046], wherein Williams indicates that a device under test (DUT) may comprise an LFSR, SEL and IC Block. *See*, 5/8/2008 Office Action, p. 6, sec. 10.col. 4, lines 5-20. Appellants respectfully disagree. Although Williams discloses that a DUT may comprise an LSFR, SEL and IC Block, Williams does not indicate that the required memory needed to execute a plurality of test vectors should be determined on a per board basis. Appellants therefore assert that Williams does not teach the limitations of claim 3.

With respect to claim 4, the Examiner refers to Williams' disclosure in paragraph [0035], wherein Williams indicates that a tester may be coupled to a DUT via a well known multi-pin test access port. However, Williams does not indicate that the required memory needed to execute a plurality of test vectors should be

determined on any sort of per pin basis. Appellants therefore assert that Williams does not teach the limitations of claim 4.

Claims 3 & 4 are believed to be allowable for at least the above reasons, and because Ohara fails to disclose that which is missing from Williams.

Claims 10 & 11 are believed to be allowable, at least, for reasons similar to why claims 3 & 4 are believed to be allowable.

Claims 15 & 16 are believed to be allowable, at least, for reasons similar to why claims 3 & 4 are believed to be allowable.

C. Claims 6, 7 & 17:

Claims 6 & 7 are believed to be allowable, in one respect, because they depend from claim 1. Claim 6 is also believed to be separately allowable, because it recites a specific method for determining the required memory for executing a plurality of test vectors, which method is not taught by Williams or Ohara.

Appellants' claim 6 recites:

> 6. The method of claim 1, wherein determining a required memory comprises:
> determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file;
> setting the required memory equal to the first memory requirement; and
> for each additional pin of the tester,
> determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and
> if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement.

The Examiner asserts that the steps of claim 6 are taught by Williams in paragraphs [0035]-[0036], which state:

> [0035] FIG. 2 illustrates a tester 14 in accordance with one embodiment of the present invention. Tester 14 is coupled to DUT 16 using well known multi-pin

test access ports. Tester 14 includes a first memory (memory1) 210 for containing a mask vector. The mask vector is generated by the ATPG tool 12 and contains a sequence of bits. The mask vector contains a respective bit for each data point of the test patterns, e.g., the mask vector contains D+R bits (when not compressed). The bits of the mask vector indicate if the corresponding test pattern data point is deterministic or random in its source. In one embodiment, a "0" in the mask vector indicates a deterministic data source and a "1" in the mask vector indicates a random data source. It is appreciated that these logic value assignments can also be reversed. An exemplary uncompressed portion of a mask vector is illustrated below:

mask 13 vector={0 0 0 0 1 1 1 1 1 1 . . . }

[0036] This indicates that the corresponding test pattern data points include four deterministic data points followed by six randomly generated points. By removing the random data from the stored test pattern and creating a mask vector, as described above, the present invention is readily able to compress the stored mask vector because it is very regular in pattern. It is appreciated that any of a number of well known methods can be used to perform data compression on the stored mask vector. However, compressing the mask vector is optional. If the mask vector is compressed, then a decompressor 215 is required to decompress the mask vector before it is used in accordance with the present invention.

Having reviewed the above text in detail, appellants cannot find any teaching or suggestion of the steps of their claim 6. Claim 6 is therefore believed to be allowable for this additional reason.

Claim 7 is believed to be allowable for the additional reason that it depends from claim 6.

Claim 17 is believed to be allowable, at least, for reasons similar to why claim 6 is believed to be allowable.

3. Conclusion

In summary, the art of record does not teach nor suggest the subject matter of appellant's claims 1-17. These claims are therefore believed to be allowable.

Respectfully submitted,
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Claims Appendix

1. A machine-executable method comprising:

reading a test file having a plurality of test vectors;

determining a required memory needed to execute the plurality of test vectors; and

using the required memory to estimate a cost to execute the test vectors.

2. The method of claim 1, further comprising receiving a billing scheme and wherein using the required memory to estimate a cost includes using the billing scheme to estimate the cost to execute the test vectors.

3. The method of claim 1, wherein determining a required memory comprises determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board.

4. The method of claim 1, wherein determining a required memory comprises determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin.

5. The method of claim 1, wherein determining a required memory comprises counting the number of test vectors for each of one or more tests in the test file.

6. The method of claim 1, wherein determining a required memory comprises:

determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file;

setting the required memory equal to the first memory requirement; and

for each additional pin of the tester,

determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and

if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement.

7. The method of claim 6, further comprising for each additional test in the test file:

for each pin of the tester, determining a third memory requirement for the pin to execute the test vectors for the additional test; and setting the required memory equal to the third memory requirement if the third memory requirement is greater than the required memory.

8. A system comprising:

logic to read a test file having a plurality of test vectors and to determine a required memory needed to execute the plurality of test vectors; and

a billing predictor, communicatively coupled to the logic, to use the required memory to estimate a cost to execute the test vectors.

9. The system of claim 8, further comprising a user interface to display the cost to a user.

10. The system of claim 8, wherein the tester includes a plurality of boards, and wherein the logic is to determine a required memory needed for each board of a tester to execute the test vectors for the board.

11. The system of claim 8, wherein the tester includes a plurality of boards, each board including a plurality of pins; and wherein the logic is to determine a required memory needed for each pin to execute the test vectors for the pin.

12. The system of claim 8, wherein the logic is to determine the required memory by counting the number of test vectors for each test in the test file.

13. One or more machine-readable mediums having stored thereon sequences of instructions, which, when executed by a machine, cause the machine to perform the actions:

reading a test file having a plurality of test vectors;

determining a required memory needed to execute the plurality of test vectors; and

using the required memory to estimate a cost to execute the test vectors.

14. The machine-readable mediums of claim 13, further comprising instructions, which when executed by the machine, cause the machine to perform the actions of receiving a billing scheme; and wherein the instructions for using the required memory to estimate a cost include instructions, which when executed by the machine, cause the machine to perform the actions of using the billing scheme to estimate the cost to execute the test vectors.

15. The machine-readable mediums of claim 13, wherein the instructions for determining a required memory comprise instructions, which when executed by the machine, cause the machine to perform the actions of determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board.

16. The machine-readable mediums of claim 13, wherein the instructions for determining a required memory comprise instructions, which when executed by the machine, cause the machine to perform the actions of determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin.

17. The machine-readable mediums of claim 13, wherein the instructions for determining a required memory comprise instructions, which when executed by the machine, cause the machine to perform the actions:

determining a first memory requirement needed for a first pin of a tester to

execute the test vectors for a first test in the test file;

setting the required memory equal to the first memory requirement; and

for each additional pin of the tester,

determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and

if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement.

Evidence Appendix

None.

Related Proceedings Appendix

None.